LU Dongzhuyuan

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EDUCATION

University of Waterloo *September 2024 - Present*
M.Eng., Electrical and Computer Engineering
CGPA: 90.5/100

The Chinese University of Hong Kong, Shenzhen *September 2019 - July 2023*
B.Eng., Electronic Information Engineering, Stream: Computer Engineering
CGPA: 3.628/4, **MGPA:** 3.668/4
Degree: *B.Eng. with Honours, First Class*
Honors & Awards: *Dean's List Award of AY2022-23, AY2021-22* and *AY2020-21*

RESEARCH EXPERIENCE

The Chinese University of Hong Kong, Shenzhen *December 2023 - June 2024*
Research Assistant at Future Network of Intelligence Institute

- Built a navigation module on the habitat-sim virtual environment which integrates a top-down 2D semantic map (based on home-robot) and a Multimodal LLM (e.g. LISA) to segment and project a short-term navigation goal captured in a RGB image to a pixel coordinate on the 2D semantic map

INTERN EXPERIENCE

KUKA Robotics (China), Midea Group *May - July 2022*
Software Development Intern, Department of Logistic Automation

- Developed the Pacecat lidar interface (specifically, ros2-based publisher node and subscriber node to process the lidar data) of the 600ic-ul Autonomous Mobile Robot (AMR)
- Designed basic high-level robot task diagrams based on Kuka Studio and Kuka RCS system and conducted tests including auto-charging, auto-lifting of the shelves, and auto-navigation

COURSE PROJECTS

Self-Trained Decision Transformer *September - December 2024*

- Collected offline reinforcement learning data from the racetrack-v0 environment based on HighwayEnv using a pre-trained Proximal Policy Optimization (PPO) model
- Proposed a framework that trains a Decision Transformer (DT) using a dataset with part of its data collected by the DT itself to address the issue when data is scarce
- Our experimental evaluation suggests that the proposed framework achieves better performance than the original DT in racetrack-v0

AthenaLite: Investigating the Training of Reasoning Abilities in Small Language Models
January - May 2023

- Prompted GPT-4 to create several templates along with an answer for math problems logically with rigorous steps on various datasets. To be more specific, a major part of our prompt is "*Can you generate a template solution for the problem without numbers?*"
- Performed few-shot prompting by feeding the question-template-answer pairs back to GPT-4 to

generate more templated aligned with human preferences on benchmarks for different math problems such as GSM8K and Proofpile

- Finetuned Aplaca-7B with the template-answer pairs based on Low-Rank Adaptation (LoRA) method and evaluated its performance on various math datasets

Self-Supervised Federated Learning on Non-iid Data *September - December 2022*

Final Year Project, Supervised by Prof. Xiaoying Tang

- Apply contrastive self-supervised learning technique including SimCLR, BYOL, and SimSiam to perform image classification task on CIFAR-10 and CIFAR-100 in a federated-learning setting with Dirichlet sampling
- Conduct experiments on personalized self-supervised federated learning method by introducing an additional l_2 loss function to each client with a regularizer to minimize the distance between the global model and local model

Database Management System Implementation *October - December 2022*

- Collaboratively implemented a miniature relational database management system (DBMS) that stores tables of data, where a table consists of some number of labeled columns of information
- Our system uses very restricted dialect of Structured Query Language (SQL) and accepts a sequence of commands from the standard input in the terminal for data insertion and extraction. The functionalities we support include create, load, insert, select from multiple tables with conditions, order by columns, case insensitivity, syntax and syntactic errors recognition, etc.

MIPS Assembler and 5-Pipelined CPU *January - May 2021*

- Built up a 5-pipelined CPU that interprets machine code, performs arithmetic operations, and stores and loads data in Verilog in the main memory. The CPU mainly consists of an arithmetic logic unit (ALU), a control unit and a main memory
- Devised a virtual MIPS instruction set architecture (ISA) assembler and simulator which “translate” assembly language into machine codes and execute them in C